REMARKS

The office action of September 6, 2002, has been carefully considered and this paper is responsive thereto. Reconsideration and allowance of the subject application are respectfully requested. Claims 3 and 4 have been amended.

While the first page of the office action lists claim 5 as being non-elected, Applicants submit that it is presented for examination (as evidenced by the rest of the office action).

Claims 1, 2, and 5 stand rejected. Claims 3 and 4 have been objected to as containing allowable subject matter.

Applicants cancel claims 1, 2, and 5 and rewrite claims 3 and 4 in independent form with substantially the same recitations as previously examined.

New claim 21 recites capacitor structures and electric fuse elements. The impurity diffusion layer, which gives rise to one of the electrodes of the fuse element is formed by impregnating an impurity via the second gate insulating film into the semiconductor substrate. The dielectric breakdown resistance of the second gate insulating layer is controlled by the impurity passing through the second gate insulating film. These features are not found in Jpn. Pat. Appln. KOKAI Publication No. 5-211221.

Applicants therefore submit this application is in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned to further prosecution.

Respectfully submitted,

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Dated: December 6, 2002

MARKED-UP VERSION TO SHOW CHANGES

IN THE SPECIFICATION:

Please delete the paragraph on page 8 beginning on line 12.

~~The present invention was made in consideration of the above situation. Accordingly, an object of the present invention is to provide an electric fuse whose performance can be controlled independent of an essential circuit element, and a method for manufacturing the same.~~

Please amend the paragraph on page 8, beginning on line 18 as follows:

~~The above object is achieved by a semiconductor device comprising~~A semiconductor device according to an aspect of the present invention comprises:

Please amend the paragraphs on page 8, beginning on line 18 as follows:

~~The above object is achieved by a semiconductor device comprising:~~

~~capacitor structures, each having a first lower electrode, a first insulating film formed on the first lower electrode and a first upper electrode formed on the first insulating film; and~~

~~electric fuse elements, each having a second lower electrode, a second insulating film formed on the second lower electrode and having an impurity concentration higher than that of the first insulating film, and a second upper electrode formed on the second insulating film, the electric fuse elements having substantially same structure as that of the capacitor structures, and being formed on same level as that of the capacitor structures, wherein information is written in the electric fuse element depending on whether the second insulating film is dielectrically broken down, and a writing voltage of the electric fuse element is determined by dielectric breakdown resistance of the second insulating film which depends on the impurity concentration of the second insulating film~~ A semiconductor device comprising:

capacitor structures, each having a first gate insulating film formed on a semiconductor substrate of a first conductivity type, and a first gate electrode formed on the first gate insulating film; and

electric fuse elements, each having a second gate insulating film formed on the semiconductor substrate and having an impurity concentration higher than that of the first gate insulating film, and a second gate electrode formed on the second gate insulating film, wherein information is written in the electric fuse element depending on whether the second gate insulating film is dielectrically broken down, and a writing voltage of the electric fuse element is determined by dielectric breakdown resistance of the second gate insulating film which depends on the impurity concentration of the second gate insulating film; and

further comprising an impurity diffusion layer of a second conductivity type, which is formed in at least a portion of the semiconductor substrate, the impurity diffusion layer being paired with the second gate electrode and serving as one electrode of the electric fuse element.

Please delete the paragraphs on page 9, beginning on line 13:

~~The above object is also achieved by a semiconductor device comprising:~~

~~capacitor structures, each having a first gate insulating film formed on a semiconductor substrate of a first conductivity type, and a first gate electrode formed on the first gate insulating film; and~~

~~electric fuse elements, each having a second gate insulating film formed on the semiconductor substrate and having an impurity concentration higher than that of the first gate insulating film, and a second gate electrode formed on the second gate insulating film, wherein information is written in the electric fuse element depending on whether the second gate insulating film is dielectrically broken down, and a writing voltage of the electric fuse element is~~

~~determined by dielectric breakdown resistance of the second gate insulating film which depends on the impurity concentration of the second gate insulating film.~~

Please amend the paragraph on page 10, beginning on line 4 as follows:

~~Further, the object of the present invention is achieved by a method for fabricating an electric fuse comprising the steps of~~A method for fabricating an electric fuse according to an aspect of the present invention comprises:

Please delete the paragraphs on page 10, beginning on line 15:

~~The object of the present invention is also achieved by a method for fabricating a semiconductor device comprising the steps of:~~

~~forming a gate insulating film on first and second regions of a semiconductor substrate of a first conductivity type;~~

~~forming a first gate electrode layer on the gate insulating film; and~~

~~injecting by ion injection an impurity into a portion of the gate insulating film on the second region of the semiconductor substrate, thereby controlling dielectric breakdown resistance of the gate insulating film on the second region to set a writing voltage of an electric fuse comprising the second region of the semiconductor substrate, the gate insulating film located on the second region and the portion of the first gate electrode layer on the second region.~~

~~The object of the present invention is also achieved by a method for fabricating a semiconductor device comprising the steps of:~~

~~forming a gate insulating film on first and second regions of a semiconductor substrate of a first conductivity type;~~

~~forming a first gate electrode layer on the gate insulating film; and~~

injecting an impurity into the second region of the semiconductor substrate in contact with the gate insulating film by ion injection through the first gate electrode layer and the gate insulating film on the second region of the semiconductor substrate, thereby forming an impurity diffusion layer, controlling dielectric breakdown resistance of the gate insulating film on the second region to set a wiring voltage of an electric fuse comprising the second region of the semiconductor substrate, the gate insulating film located on the second region and the first gate electrode layer located on the second region.

The object of the present invention is also achieved by a method for fabricating a semiconductor device comprising the steps of:

forming a gate insulating film on first and second regions of a semiconductor substrate;

forming a first gate electrode layer on the gate insulating film;

patterning the first gate electrode layer, thereby forming gate electrodes of MOS transistors on the first region of the semiconductor substrate, and electric fuses of a capacitor structure, each having the semiconductor substrate, the gate insulating film and the first gate electrode layer on the second region; and

injecting by ion injection an impurity from a direction obliquely with respect to a normal of the semiconductor substrate into a portion of the semiconductor substrate exposed by patterning the first gate electrode layer and a portion of the semiconductor substrate immediately under an edge portion of the first gate electrode layer in the second region, thereby forming an impurity diffusion layer serving as one electrode of an electric fuse, the ion injection causing the impurity to pass through the gate insulating film or to be injected into the gate insulating film, thereby controlling dielectric breakdown resistance of the gate insulating film to set a writing voltage of the electric fuse.

~~Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.~~

Please delete the paragraph on page 13, beginning on line 8:

~~The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently embodiments of the invention, and together with the general description given above and the detailed description of the embodiments given below, serve to explain the principles of the invention.~~

Please amend the paragraph on page 35, beginning on line 1 as follows:

In the embodiments described above, the anti-fuse utilizes a part of the cell capacitor or the MOS transistor of a DRAM. However, ~~the gist of~~ the embodiment of the present invention is to control the dielectric breakdown resistance by introducing an impurity into the insulating film of the anti-fuse. Therefore, the embodiment of the present invention is not limited to the structures of the first to fifth embodiments. Other structures of the embodiments will be described below.

Please amend the paragraph on page 16, beginning on line 22 as follows:

Thereafter, an impurity diffusion layer of a MOS transistor and an interlayer insulating film covering the MOS transistor are formed by the known technique. As a result, a semiconductor device is completed. In the semiconductor device as shown in FIG. 3C, a fuse capacitor comprising the silicon substrate 30, the gate insulating film 32b doped with the impurity and the gate electrode 33 ~~constitutes~~forms an anti-fuse.

Please amend the paragraph on page 19, beginning on line 2 as follows:

Thereafter, a resist 50-2 is formed on the silicon substrate 30, and then patterned to expose only a portion of the peripheral region by means of lithography. Then, as shown in FIG. 4B, an n-type impurity is ion-injected. The acceleration voltage at the ion injection is adjusted so that the impurity ions can be implanted into the gate insulating film 32a and the silicon substrate 30 through the tungsten film 33b and the polycrystalline silicon film 33a. Through this step, a gate insulating film 32b doped with the impurity is formed in the peripheral region A4, and an n-type impurity diffusion layer 51 is formed in the silicon substrate 30. As described above, the gate electrode 33 in the peripheral region A4 is displaced from the element region. Therefore, the impurity diffusion layer 51 formed in the silicon substrate 30 ~~is constituted by~~includes two impurity diffusion layers 51a and 51b of different depths. In other words, due to the ions passing through the gate electrode 33, the impurity diffusion layer 51b formed immediately under the gate electrode 33 is shallower than the impurity diffusion layer 51a, which is not covered by the gate electrode 33.

Please amend the paragraph on page 35, beginning on line 14 as follows:

FIG. 9A shows an anti-fuse using an interlayer insulating film. As shown in FIG. 9A, a polycrystalline silicon film 33a and a tungsten film 33b, ~~constituting~~serving as a gate electrode 33, are formed on a gate insulating film 32a, which is formed on a silicon substrate 30. An interlayer insulating film 52 is formed on the tungsten film 33b. A metal wiring layer 54 including a barrier metal layer 54a and a metal layer 54b is formed on the interlayer insulating film 52. This structure constitutes an anti-fuse in which the gate electrode 33 and the metal wiring layer 54 serve as capacitor electrodes and the interlayer insulating film 52 serves as a

capacitor insulating film. The dielectric breakdown resistance, i.e., the writing voltage, of the anti-fuse can be controlled by ion-injecting an impurity into the interlayer insulating film 52 serving as the capacitor insulating film.

Please amend the paragraph on page 36, beginning on line 5 as follows:

FIG. 9B shows an anti-fuse using a gate sidewall insulating film. As shown in FIG. 9B, a gate electrode 33 is formed on a silicon substrate 30 with a gate insulating film 32a interposed therebetween. A gate sidewall insulating film 55 covering the gate electrode 33 is provided. A metal wiring layer 56 abuts on the gate sidewall insulating film 55. This structure ~~constitutes~~forms an anti-fuse in which the gate electrode 33 and the metal wiring layer 56 serve as capacitor electrodes and the gate sidewall insulating film 55 serves as a capacitor insulating film. The dielectric breakdown resistance, i.e., the writing voltage, of the anti-fuse can be controlled by ion-injecting an impurity into the gate sidewall insulating film 55 serving as the capacitor insulating film.

Please amend the paragraph on page 36, beginning on line 20 as follows:

FIG. 9C shows an anti-fuse using an insulating film interposed between metal wiring layers. As shown in FIG. 9C, two metal wiring layers 57 are buried in an interlayer insulating film 52. An anti-fuse ~~is constituted by~~includes the metal wiring layers 57 serving as capacitor electrodes, and the portion of the interlayer insulating film 52 located between the two wiring layers 57, which serves as a capacitor insulting film. The dielectric breakdown resistance, i.e., the writing voltage, of the anti-fuse can be controlled by ion-injecting an impurity into the portion of the interlayer insulating film 52 located between the two metal wiring layers 57.

IN THE CLAIMS:

Claims 1, 2, and 5 have been deleted. Claims 3 and 4 are amended as follows:

3. (Amended) A semiconductor device comprising:

capacitor structures, each having a first gate insulating film formed on a semiconductor substrate of a first conductivity type, and a first gate electrode formed on the first gate insulating film; and

electric fuse elements, each having a second gate insulating film formed on the semiconductor substrate and having an impurity concentration higher than that of the first gate insulating film, and a second gate electrode formed on the second gate insulating film, wherein information is written in the electric fuse element depending on whether the second gate insulating film is dielectrically broken down, and a writing voltage of the electric fuse element is determined by dielectric breakdown resistance of the second gate insulating film which depends on the impurity concentration of the second gate insulating film; and ~~The semiconductor device according to claim 2,~~

~~further comprising~~ an impurity diffusion layer of a second conductivity type, which is formed in at least a portion of the semiconductor substrate ~~and which abuts on the second gate insulating film under the second gate electrode~~, the impurity diffusion layer being paired with the second gate electrode and serving as one electrode of the electric fuse element.

4. (Amended) A semiconductor device comprising:

capacitor structures, each having a first gate insulating film formed on a semiconductor substrate of a first conductivity type, and a first gate electrode formed on the first gate insulating film; and

electric fuse elements, each having a second gate insulating film formed on the semiconductor substrate and having an impurity concentration higher than that of the first gate insulating film, and a second gate electrode formed on the second gate insulating film, wherein